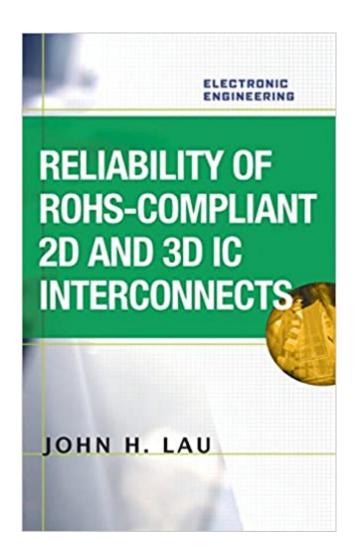


The book was found

Reliability Of RoHS-Compliant 2D And 3D IC Interconnects (Electronic Engineering)





Synopsis

Proven 2D and 3D IC lead-free interconnect reliability techniques Reliability of RoHS-Compliant 2D and 3D IC Interconnects offers tested solutions to reliability problems in lead-free interconnects for PCB assembly, conventional IC packaging, 3D IC packaging, and 3D IC integration. This authoritative guide presents the latest cutting-edge reliability methods and data for electronic manufacturing services (EMS) on second-level interconnects, packaging assembly on first-level interconnects, and 3D IC integration on microbumps and through-silicon-via (TSV) interposers.

Design reliable 2D and 3D IC interconnects in RoHS-compliant projects using the detailed information in this practical resource. Covers reliability of: 2D and 3D IC lead-free interconnects CCGA, PBGA, WLP, PQFP, flip-chip, lead-free SAC solder joints Lead-free (SACX) solder joints Low-temperature lead-free (SnBiAg) solder joints Solder joints with voids, high strain rate, and high ramp rate VCSEL and LED lead-free interconnects 3D LED and 3D MEMS with TSVs Chip-to-wafer (C2W) bonding and lead-free interconnects Wafer-to-wafer (W2W) bonding and lead-free interconnects Wafer-to-wafer (W2W) bonding and lead-free interconnects Electromigration of lead-free microbumps for 3D IC integration

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Customer Reviews

John H. Lau, Ph.D., P.E., IEEE Fellow, ASME Fellow, ITRI Fellow, spent 30 years in the electronics industry (HP and Agilent) in Palo Alto, California, and currently serves as a fellow at the Electronics & Optoelectronics Laboratories, Industrial Technology Research Institute (ITRI), Taiwan. He has

published 15 books with McGraw-Hill, including Advanced MEMS Packaging, Electronics Manufacturing with Lead-Free Solders and Low Cost Flip Chip Technologies.

This is an excellent reference book for students in senior level or graduate school to understand the advanced packaging related knowledge, including reliability, and a useful tool for engineers in their work on advanced packaging design and analysis. The book covers a wide spectrum with focus on basic concepts and case studies for various advanced electronic and photonic packaging products. In addition, this book, as one of very few in the market, addresses TSV-based 3D IC/Si integration reliability issues. 3D IC/Si integration is the mainstream for semiconductor packaging technology evolvement as it enables the technology to migrate beyond the Moore's Law. Handling 3D packaging reliability is always much more challenging compared to the 2D packaging solutions. I am glad to see that this book addresses both 2D and 3D IC packaging/integration issues and is written by an expert who has been active in the semiconductor field for over 30 years.

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